

STACKING STRUCTURE OF SEMICONDUCTOR CHIPS AND SEMICONDUCTOR PACKAGE USING IT

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FIELD OF THE INVENTION

The present invention relates to semiconductor chips, and more particularly, to a stacking structure of semiconductor chips and a semiconductor package using it in which a conductive wire can be electrically insulated while a conductive wire is contacted with a lower surface of an upper semiconductor chip thereby preventing mechanical damage of the wire, and also diminishing a total thickness of the stacking structure.

BACKGROUND OF THE INVENTION

As electronic devices get smaller, the components within these devices must get smaller as well. Because of this, there has been an increased demand for the miniaturization of components and greater packaging density. Integrated Circuit (IC) package density is primarily limited by the area available for die mounting and the height of the package. One way of increasing the density is to stack multiple die vertically in an IC package. Stacking multiple die will maximize function and efficiency of the semiconductor package.

In order to stack multiple die vertically in an IC package, an adhesive layer is required between the vertically stacked die. However, presently stacked IC packages require an extraordinarily thick adhesive layer between each die. The thick adhesive layer is necessary in order to prevent the conductive wire of the lower die from contacting the bottom surface of the upper die thereby preventing an electrical short. Unfortunately, the thickness of the adhesive layer limits the number of die that may be vertically stacked in the IC package.

Therefore, a need existed to provide a device and method to overcome the above problem.

SUMMARY OF THE INVENTION

A semiconductor package and a method of producing the same has a substrate. A first semiconductor chip is coupled to a surface of the substrate. The first semiconductor chip has a first and second surfaces which are substantially flat in nature. An adhesive layer is coupled to the second surface of the first semiconductor chip. A second semiconductor chip having first and second surfaces which are substantially flat in nature is further provided. An insulator is coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds. The second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.

The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a sectional view of one embodiment of the present invention;

FIG. 1A and 1B are magnified views of circle I as shown in FIG. 1;

FIG. 2 illustrates a sectional view of another embodiment of the present invention;

FIG. 2A and 2B are magnified views of circle II as shown in FIG. 2;

FIG. 3 illustrates a sectional view of another embodiment of the present invention;

FIG. 3A and 3B are magnified views of circle III as shown in FIG. 3;

FIG. 4 illustrates a sectional view of another embodiment of the present invention;

FIG. 4A is a magnified view of circle IV as shown in FIG. 4;

FIG. 5 illustrates a sectional view of another embodiment of the present invention;

FIG. 6 illustrates a sectional view of another embodiment of the present invention; and

FIG. 7 illustrates a sectional view of another embodiment of the present invention.

Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

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DETAILED DESCRIPTION

Referring to FIG. 1, a sectional view of one embodiment of the present invention is shown. FIG.1 illustrates a stacking structure 11 of a semiconductor chip wherein a substrate 7 having a substantially plate form, is provided. As is generally known, a printed circuit board, a circuit tape, a circuit film, a lead frame or the like may be used as the substrate 7. This is only a matter of selection by a person skilled in the art, and, therefore, this does not adversely influence the present invention.

As shown in FIG. 1, a first semiconductor chip 1 is bonded on a top surface of the substrate 7. The semiconductor chip 1 includes a first surface 1a and a second surface 1b, which are substantially flat in nature. A plurality of input-output pads 1c are formed on the second surface 1b of the first semiconductor chip 1.

There is an edge pad type semiconductor chip 1 in which a plurality of input-output pads 1c are formed at the inner circumference of the second surface 1b. A center pad type semiconductor chip will be described with reference to FIG. 4 hereafter.

An adhesive layer 3 having a predetermined thickness is bonded on the inside of the second surface 1b of the first semiconductor chip 1, excluding the input-output pads 1c. The adhesive layer 3 may include such substances as a nonconductive liquid phase adhesive, a nonconductive adhesive tape or other substances that are commonly known in the art for semiconductor chip attachment.

The adhesive layer 3 serves as an adhesive bonding to the second semiconductor chip 2 on the second surface 1b of the first semiconductor chip 1. Here, it is possible for the adhesive layer 3 to be formed in the same thickness as a loop height of a first conductive wires 5 mentioned below or a smaller thickness than the loop height. However, when the thickness of the adhesive layer 3 is thinner than the loop height, it is desirable that the thickness of the adhesive layer 3 is to be more than about 80% of the loop height. This will be described in detail hereafter.

Continuously, the input-output pads 1c of the first semiconductor chip 1 and the substrate 7 can be bonded to each other by the first conductive wires 5, such as gold or copper or aluminum wires or by its equivalent. This is performed by a conventional normal wire bonding manner which will be described hereafter. It should be noted that the listing of the different types of wires is just used as an example and should not be seen as to limit the scope of the present invention.

Continuously, a second semiconductor chip 2 having a first surface 2a and a second surface 2b, which are substantially flat in nature, is placed on the upper part of the adhesive layer 3. A plurality of input-output pads 2c are formed on the second surface 2b of the second semiconductor chip 2.

An insulator 4 is formed on the first surface 2a of the second semiconductor chip 2. That is, the insulator 4 formed on the first surface 2a of the second semiconductor chip 2 is bonded on the upper part of the adhesive layer 3.

The insulator 4 may include such substances as a liquid phase adhesive, an adhesive tape/film, a polyimide, an oxide layer and a nitride layer or other substances that are commonly known in the art for semiconductor chip or package. It is desirable that all these insulators have a nonconductive, soft, and elastic nature. Also, it is desirable that the thickness of the insulator 4 may be more than about 20% of the loop height of the first conductive wires 5.

The insulator 4, but not limited to, is formed in a wafer state before separating into individual semiconductor chips. That is, the insulator 4 can be formed by bonding the nonconductive tape/film on the back surface of the wafer, or by coating the nonconductive liquid phase adhesive or the polyimide on the back surface of the wafer in a spin coating or in a spray manner. Also, the insulator 4 can be formed by evaporating a relatively thicker oxide layer or nitride layer on the back surface of the wafer.

After forming the nonconductive tape/film, nonconductive liquid phase adhesive, polyimide, oxide layer or nitride layer (insulator) on the back surface of the wafer, a plurality of semiconductor chips are separated from the wafer, respectively.

5 Alternatively, insulator 4 may be formed at the individual semiconductor chip which is already separated from the wafer. Namely, after the semiconductor chip is separated from the wafer, the insulator 4 is formed at back surface of the semiconductor chip as described above.

10 As mentioned above, after forming insulator 4 on the first surface 2a of the second semiconductor chip 2, the second chip 2 is compressed and adhered to the upper part of adhesive layer 4.

15 At this time, since thickness of the adhesive layer 3 may be about the same or thinner than the loop height of the first conductive wires 5, the first conductive wires 5 may be contacted with the insulator 4 formed at the first surface 2a of the second semiconductor chip 2. However, the loop height portion of the first conductive wires 5 exposed outward from adhesive layer 3 is
20 about 20% of total loop height in the first conductive wires 5. And thickness of the insulator 4 is more than 20% of the total loop height of the first conductive wires 5. Thus, the first conductive wires 5 do not directly contact to the first surface 2a of the second semiconductor chip 2.

Even in the case that the loop height portion of the first conductive wires 5 become exposed outward from adhesive layer 3, the first conductive wires 5 do not directly contact to the first surface 2a of the second semiconductor chip 2 by the insulator 4. Also, since the insulator 4 has a nonconductive, soft, and elastic nature, the first conductive wires 5 have no electrical or mechanical damages. Namely, the first conductive wires 5 can be easily overlapped or superimposed with the insulator 4 and the conductive wires 5 can be independent in the insulator 4. Thus, the first conductive wires 5 do not short each other and aren't heavily damaged by the insulator 4. The tape/film as the insulator 4 seems to have the most soft and elastic nature among the insulator mentioned above.

An edge pad type semiconductor chip 2, in which a plurality of input-output pads 2c is formed at the inner circumference of the second surface 2b, is illustrated in the FIG. 1. However, a center pad type semiconductor chip 2, in which a plurality of input-output pads 2c is formed at the center of the second surface 2b, can also be used.

Continuously, the input-output pads 2c of the second semiconductor chip 2 and the substrate 7 can be bonded to each other by the second conductive wires 6, as described above or its equivalent.

As shown in FIG. 1A and 1B, which is a magnified view of circle I as shown in FIG. 1, the above conventional normal wire bonding is constructed in such a manner that an end of the

conductive wire 5 is bonded on the input-output pad 1c of the semiconductor chip 1 by conductive ball 51(ball bonding). Then the other end of the conductive wire 5 is bonded on the substrate 7 by stitch bonding.

5 As shown in FIG. 1A, if the adhesive layer 3 does not cover the input-output pads 1c, the wire bonding can be performed selectively before or after formation of the adhesive layer 3.

10 However, as shown in FIG. 1B, if adhesive layer 3 covers the input-output pads 1c, then the wire bonding must be performed before forming the adhesive layer 3. Here, if the adhesive layer 3 covers the input-output pads 1c of the semiconductor chip 1, the nonconductive liquid phase adhesive as adhesive layer 3 is generally used. That is, the adhesive tape as adhesive layer 3 may affect damages in the first conductive wires 5.

15 According to the stacking structure 11 of the present invention, the first conductive wires 5 are not directly contacted with the first surface 2a of the semiconductor chip 2. Thus, the phenomenon of an electrical short will not occur. Furthermore, mechanical damage of the first conductive wires 5 can also be prevented. Though the first conductive wires 5 are contacted with the insulator 4, electrical or mechanical damage has never occurred. That is, because of a nonconductive, soft and elastic nature of insulator 4, the first conductive wires 5 can be easily overlapped or superimposed with the insulator 4 and the conductive wires 5 can be independent in the insulator 4. Thus, the first conductive wires 5 do not short each other and aren't heavily

damaged by the insulator 4.

Also, the thickness of the adhesive layer 3 can adequately become thinner. Namely, in prior art, the adhesive layer 3 should be formed in substantially twice the thickness of the loop height of the first conductive wires 5. However, in the present the invention, the adhesive layer 3 can be formed in the same thickness as the loop height of the first conductive wires 5 or a thickness that is less than the loop height. Thus, this invention can diminish a total thickness of the stacking structure of the semiconductor chips.

Referring to FIG. 2, a sectional view of another embodiment of the present invention is illustrated. Referring also to FIG. 2A and 2B, magnified views of circle II shown in FIG. 2 are also illustrated. Since a stacking structure 12 illustrated in FIG. 2 is constructed in a similar manner to the stacking structure of FIG. 1, only differences existing there between will be described herein below.

As shown in FIG. 2 or FIG. 2A, the first and the second conductive wires 5 and 6 are not formed from a conventional normal bonding manner. Instead, a reverse bonding manner is used. Namely, the conventional normal bonding is constructed in such a manner that an end of the conductive wire is bonded on the input-output pad of the semiconductor chip by ball bonding. The other end of the conductive wire is then bonded on the substrate by stitch bonding.

Meanwhile, the reverse bonding is constructed in such a manner that an end of the conductive wire 5 is bonded on the substrate by conductive ball 51' (ball bonding). Then the other end of the conductive wire 5 is bonded on the input-output pad 1c of the semiconductor chip 1 by stitch bonding. Of course, a conductive ball 51 is formed on the input-output pads of semiconductor chip 1 by the conductive wire 5 in advance in order to alleviate an impulse created by the stitch bonding. The reverse bonding can be applied to all the first and second conductive wires 5 and 6 by which the first semiconductor chip 1 and the second semiconductor chip 2 are connected to the substrate 7, respectively.

In the case where the reverse bonding is used, the thickness of the adhesive layer 3 can be thinner owing to a lower loop height of the first conductive wires 5. That is, as the loop height of the conductive wire 5, which is bonded by the stitch bonding, is very low, the thickness of the adhesive layer 3 can be reduced sharply.

Also, since the loop height of the conductive wires 5 is low, when the second semiconductor chip 2 is adhered or compressed to the adhesive layer 3, the first conductive wires 5 have less mechanical stress than the first embodiment. Thus, the first conductive wires 5 can not create an electrical short or mechanical damage.

In certain cases, the insulator 4 having elevated bonding power can be used as bonding materials without using the adhesive layer 3. Nevertheless, since the insulator 4 has the nonconductive, soft and elastic nature, the first conductive wires 5 can not create an electrical short or mechanical damage.

Of course, the adhesive layer 3 may cover the input-output pads 1c of the first semiconductor chip 1 (not shown) and the second conductive wires 6 may connect between the input-output pads 2c and the substrate 7 by normal bonding.

Further, as shown in FIG.2B, a wedge bonding manner can be applied to the first and the second conductive wires 5 and 6 in order to lower the loop height. That is, the wedge bonding is constructed in such a manner that an end of the conductive wire is bonded on the input-output pad of the semiconductor chip by stitch bonding. Then, the other end of the conductive wire is bonded on the substrate by stitch bonding.

Similarly, in the case where the wedge bonding is used, the thickness of the adhesive layer 3 can be thinner owing to a lower loop height of the first conductive wires 5. That is, as the loop height of the conductive wire, which is bonded by the stitch bonding, is very low, the thickness of the adhesive layer 3 can be reduced sharply.

Also, since the loop height of the conductive wires 5 is low, when the second semiconductor chip 2 is adhered or compressed to the adhesive layer 3, the first conductive wires 5 have less mechanical stress than the first embodiment.

Referring to FIG. 3, a sectional view of another embodiment of the present invention is illustrated. Also referring to FIG. 3A and 3B, magnified views of circle III as shown in FIG. 3 are illustrated. Since a stacking structure 13 is constructed in a similar manner to the stacking structure 12 of FIG. 2, only differences existing there between will be described herein below. As shown in FIG. 3 and 3A, the first and the second conductive wires 5 and 6 are formed by a reverse bonding manner. The conductive ball 51 is formed on the input-output pads 1c and 2c of the semiconductor chip 1 and 2 by the conductive wire in advance in order to alleviate an impulse created by the stitch bonding.

Furthermore, a supporter 52 is formed on the upper part of the conductive wires 5 connected with input-output pads 1c of the semiconductor chip 1. Namely, the supporter 52 is formed on the upper part of the conductive balls 51 and the first conductive wires 5 together. Also, the supporter 52 may be formed on the outside of the input-output pads 1c. For example, a plurality of the supporters 52 can be formed on the inner circumference of the second surface 1b of the semiconductor chip 1.

The supporter 52 may be formed after wire bonding. Namely, first of all, the conductive ball 51 is formed on the input-output pads 1c, and the first conductive wire 5 is bonded to the conductive ball 51. At last, the supporter 52 is formed on the first conductive wire 5 superimposed over the conductive ball 51.

The supporter 52 may be formed by conventional stud bump forming manner. For example, a ball is formed at end of a conductive wire, and the ball is fused to the top of the first conductive wire 5. The conductive wire is then cut off except the ball. Furthermore, another ball is formed at the end of the conductive wire, and this ball is bonded to the fused ball above mentioned. As for a repetition of this manner, as shown in FIG. 3A, a raw type conductive ball forms the supporter 52.

The supporter 52 may include such substances as gold, silver, copper, and solder or other substances that are commonly known in the art for the semiconductor chip. The above listing of substances should not be seen as to limit the scope of the present invention.

Meanwhile, the supporter 52 is contacted with the bottom of the insulator 4 formed on the second semiconductor chip 2 so as to support the second semiconductor chip 2. Thus, since the supporter 52 supports many portions of the insulator 4 formed on the semiconductor chip 2, the semiconductor chip 2 will be supported more stable. Of course, the adhesive layer 3 may cover the input-output pads 1c of the first semiconductor chip 1 and the supporter 52.

Further, as shown in FIG.3B, a wedge bonding manner can be applied to the first and the second conductive wires 5 and 6 in order to lower the loop height.

Similarly, the supporter 52 is formed on the upper part of the conductive wires 5 connected with input-output pads 1c of the semiconductor chip 1. The supporter 52 is contacted with the insulator 4 so as to support the second semiconductor chip 2. Thus, since the supporter 52 supports the insulator 4 formed on the semiconductor chip 2, the semiconductor chip 2 becomes more stable.

Also, since the conductive wires 5 is covered with supporter 52, when the second semiconductor chip 2 is adhered or compressed to the adhesive layer 3, the first conductive wires 5 have less mechanical stress than the previous embodiments.

Referring to FIG. 4, a sectional view of another embodiment of the present invention is illustrated. And referring to FIG.4A, magnified views of circle IV as shown in FIG. 4 is illustrated. Since a stacking structure 14 is constructed in a similar manner to the stacking structure 12 of FIG. 2, only differences existing there between will be described herein below.

As shown in the drawings, there is a center pad type semiconductor chip 1 in which a plurality of input-output pads 1c are formed at the center of the second surface 1b. Also, the input-output pads 1c of the first semiconductor chip 1 and the substrate 7 are bonded to each other by the reverse bonding of the first conductive wires 5.

The reverse bonding manner, as described above, has advantages in that the thickness of the adhesive layer 3 can be thinner. Furthermore, the first conductive wires 5 don't make

contact with the region except for the input-output pads 1c of the first semiconductor chip 1 without increasing the loop height.

Here, it is, but not limited to, that a nonconductive liquid phase adhesive is used as the adhesive layer 3. That is, as a certain portion of the first conductive wires 5 is positioned at the inside of the adhesive layer 3, it is desirable to use the nonconductive liquid phase adhesive rather than solid phase adhesive tape. In other words, the input-output pads 1c of the first semiconductor chip 1 and the substrate 7 is bonded to each other by the reverse bonding of the first conductive wires 5. Of course, conductive balls 51 are formed on the input-output pads 1c of the semiconductor chip 1 by the conductive wire in advance in order to alleviate an impulse created by the stitch bonding.

The nonconductive liquid phase adhesive is applied to the first surface 1a of the first semiconductor chip 1 and is hardened. Then, the second semiconductor chip 2, to which the insulator 4 is stuck, is bonded on the adhesive layer 3. The insulator 4 may include such substances as a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer and a nitride layer or other substances that are commonly known in the art for semiconductor chips or packages, as described above. Again, the listing of the above substances should not be seen as to limit the scope of the present invention.

Further, a wedge bonding can be applied to the first and the second conductive wires 5 and 6 in order to lower the loop

height. That is, the wedge bonding is constructed in such a manner that an end of the conductive wire is bonded on the substrate by stitch bonding. Then, the other end of the conductive wire is bonded on the input-output pad of the semiconductor chip by stitch bonding.

Also, in the FIG. 4, the input-output pads 2c of the second semiconductor chip 2 are bonded to substrate 7 by the reverse bonding of conductive wires 6. However, the normal bonding manner is also possible. Furthermore, the second semiconductor chip 2 of the edge pad type is illustrated in FIG. 4. However, the center pad type is also possible. In this case, the second conductive wires 6 are generally bonded to substrate 7 by the reverse bonding or wedge bonding.

Meanwhile, the stacking structures according to the present invention are described on the basis of the first and the second semiconductor chips 1 and 2. However, a plurality of semiconductor chips (for example, a third semiconductor chip, a fourth semiconductor chip, etc.) may be stacked one up on another. It will be appreciated by those persons skilled in the art that such an arrangement is optional. In other words, the present invention is not limited by a number of the stacked semiconductor chips.

Referring to FIG. 5, a sectional view of another embodiment of the present invention is illustrated. The stacking structure of the semiconductor chip is identical with that of FIG.

1. As shown in the FIG. 5, a substrate 70 having a substantially plate form is provided. The substrate 70 includes resin layer 71, a plurality of circuit patterns 72 formed at a top and bottom of the resin layer 71 and a plurality of conductive via 73 connecting the top and bottom circuit patterns 72. The substrate 70, as is generally known, may be a printed circuit board, circuit tape or circuit film. The listing of the substrates 70 should not be seen as to limit the scope of the present invention.

A first semiconductor chip 1 is bonded on a surface of the substrate 70. The semiconductor chip 1 includes a first surface 1a and a second surface 1b, which are substantially in a flat type. A plurality of input-output pads 1c are formed on the second surface 1b of the first semiconductor chip 1.

The input-output pads 1c of the first semiconductor chip 1 and some top circuit patterns 72 of the substrate 70 are bonded to each other by the first conductive wires 5.

An adhesive layer 3 having a predetermined thickness is bonded on the second surface 1b of the first semiconductor chip 1.

A second semiconductor chip 2 having a first surface 2a and a second surface 2b, which are substantially in a flat type, is positioned on the upper part of the adhesive layer 3. A plurality of input-output pads 2c are formed on the second surface 2b of the second semiconductor chip 2. Further, an insulator 4 is formed on the first surface 2a of the second semiconductor chip 2. The input-output pads 2c of the second semiconductor chip 2 and others

top circuit patterns 72 of the substrate 70 are bonded to each other by the second conductive wires 6.

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Moreover, the first semiconductor chip 1, the adhesive layer 3, the second semiconductor chip 2, insulator 4, the first and the second conductive wires 5 and 6 are sealed with sealing material, such as an epoxy molding compound. The area sealed with the sealing material is defined as a sealing part 8.

Finally, conductive balls 9 such as solder balls are fused to the bottom circuit patterns of the substrate 70. Such semiconductor package 15 can be mounted to a mother board later.

Referring to FIG. 6, a sectional view of another embodiment of the present invention is illustrated. The stacking structure of the semiconductor chip is identical with that of FIG. 1. Since the semiconductor package 16 is constructed in a similar manner to the semiconductor package 15 of FIG. 5, only differences existing there between will be described herein below.

As shown in FIG. 6, a perforating hole 74 of which size is larger than that of the semiconductor chip 1 is formed on a center of the substrate 70. A plurality of circuit patterns 72 are formed at the outside of the perforating hole 74. The semiconductor chip 1 is located in the perforating hole 75 so as to form a thinner semiconductor package 15. The input-output pads 1c of the semiconductor chip 1 are bonded to circuit patterns 72 by the first conductive wires 5.

Furthermore, the sealing part 8 is formed inside at the perforating hole 74, and the first surface 1a of the semiconductor chip 1 is exposed outward from the sealing part 8 so as to increase

the heat dissipation capability of the first semiconductor chip 1.

Since the semiconductor chip and the substrate is overlapped by each other, the total thickness of the semiconductor package 15 becomes thinner. Furthermore, since the first surface 1a of the semiconductor chip 1 is exposed outward from the sealing part 8, the semiconductor package 15 increases its heat dissipation capability.

Referring to FIG. 7, a sectional view of another embodiment of the present invention is illustrated. A stacking structure of the semiconductor chip is identical with that of FIG. 1. As shown in FIG. 7, a substrate 80 having a substantially plate form is provided. The substrate 80 includes chip mounting plate 81 and a plurality of leads 82 formed at an outside of the chip mounting plate 81. Such a substrate 80, as is generally known, may be a conventional lead frame or a micro lead frame (MLF).

A first semiconductor chip 1 is bonded to the chip mounting plate 81 of the substrate 80. The semiconductor chip 1 includes a first surface 1a and a second surface 1b, which are substantially flat in nature. A plurality of input-output pads 1c are formed on the second surface 1b of the first semiconductor chip 1. The input-output pads 1c of the first semiconductor chip 1 and some leads 82 of the substrate 80 are bonded to each other by the first conductive wires 5.

An adhesive layer 3 having a predetermined thickness is bonded on the second surface 1b of the first semiconductor chip 1.

A second semiconductor chip 2 having a first surface 2a and a second surface 2b, which are substantially flat in nature, is positioned on the upper part of the adhesive layer 3. A plurality of input-output pads 2c are formed on the second surface 2b of the second semiconductor chip 2. An insulator 4 is formed on the first surface 2a of the second semiconductor chip 2.

The input-output pads 2c of the second semiconductor chip 2 and others leads 82 of the substrate 80 are bonded to each other by the second conductive wires 6.

Moreover, the first semiconductor chip 1, the adhesive layer 3, the second semiconductor chip 2, insulator 4, the first and the second conductive wires 5 and 6, and the substrate 80 are sealed with sealing material, such as an epoxy molding compound. The area sealed with the sealing material is defined as a sealing part 8. Here, a bottom surface of the chip mounting plate 81 and plurality of leads 82 are exposed outward from the sealing part 8.

Also, these semiconductor packages 15, 16 and 17 can include the stacking structures illustrated in FIG. 2, 3 and 4. Furthermore, the stacking structure according to the present invention is described on the basis of the first and the second semiconductor chips 1 and 2. However, a plurality of semiconductor chips (for example, a third semiconductor chip, a fourth semiconductor chip, etc.) may be stacked one up on another. It will be appreciated by those persons skilled in the art that such an arrangement is optional. In other words, the present invention

is not limited by the number of the semiconductor chip.

According to the stacking structure of the semiconductor chip and the semiconductor package using it, the insulator is further formed on the first surface of the second semiconductor chip, where it can be electrically insulated while the conductive wire is contacted with the insulator.

Also, the insulator is made from a soft or elastic material, thereby preventing the mechanical damage of the conductive wire. Furthermore, the thickness of the adhesive layer can become thinner adequately in order to diminish a total thickness of the stacked semiconductor chip or package.

Moreover, the conductive wire is stuck to the insulator, thereby having the effect of preventing the leaning phenomenon of the conductive wire during the sealing process and or the like.

This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material and manufacturing process may be implemented by one of skill in the art in view of this disclosure.